IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application Serial No	10/622,295
Filing Date	
Inventor	
Assignee	Micron Technology, Inc.
Priority Group Art Unit	2824
Priority Examiner	Bradley Smith
Attorney Docket No	MI22-2342
Title: Semiconductor Constructions and Methods	of Forming Semiconductor

SEP 0 2 2003

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450 OFFICIAL

CERTIFICATE OF FACSIMILE TRANSMISSION UNDER 37 CFR § 1.8

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- Certificate of Facsimile Transmission
- Information Disclosure Statement w/PTO-1449

Dated: September 2,2003 Jaime M. White Telephone No. (509) 624-4276 Facsimile No. (509) 838-3424

NUMBER OF PAGES IN FACSIMILE: 3

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Inventor:

Joel A. Drewes

Title:

Semiconductor Constructions and Methods of Forming Semiconductor

Constructions

Assignee:

Micron Technology, Inc.

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INFORMATION DISCLOSURE STATEMENT

PURSUANT TO 37 C.F.R. §§ 1.56, 1.97 AND 1.98

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449. No admission is made regarding whether all the submitted references are prior art.

The listed references were cited by, or submitted to, the Office in the parent, co-pending application of the above-identified application. The above-identified application is a divisional application of co-pending application Serial No. 10/121,298, filed April 11, 2002. Such prior disclosure is sufficient for the above-identified application as far as copies of the references are concerned. 37 C.F.R. § 1.98(d) and MPEP § 609(2).

Citation of these references is respectfully requested.

Dated: 9/7/13

Ву:

David G. Latwesen, Ph.D.

Respectfully submitted.

Reg. No. 38,533

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